PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 23, 2004 Denise Sheridan

Date Denise Sheridan

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Joseph M. Jeddeloh	Attorney Docket No.	: 501321.01
Serial No.	: 10/660,844	Group Art Unit	: 2184
Filed	: September 12, 2003	Examiner	: Not yet assigned
Title	: SYSTEM AND METHOD FOR ON-BOARD TIMING MARGIN TESTING OF MEMORY MODULE		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

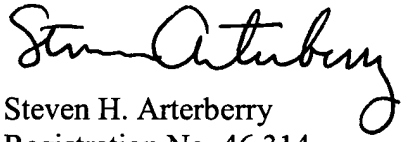
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. A copy of the cited non-patent literature reference, as required under 37 C.F.R. § 1.98(a)(2), is enclosed. Copies of the cited U.S. patents and U.S. patent application publications will not be submitted herewith in accordance with the waiver by the Office of the requirement under 37 C.F.R. § 1.98(a)(2)(i) for U.S. national patent applications filed after June 30, 2003. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

I hereby certify that no item set forth on the attached form PTO-1449 was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge, after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Please acknowledge receipt of this Supplemental Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,
DORSEY & WHITNEY LLP



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SHA:dms
Enclosures:
Postcard
Form PTO-1449
Cited References (1)

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501321.01	APPLICATION NO. 10/660,844
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) **Joseph M. Jeddeloh**	
		FILING DATE September 12, 2002	GROUP ART UNIT 2184

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,818,844	10/06/98	Singh et al.	370	463	
	AB	6,272,609	08/07/01	Jeddeloh	711	169	
	AC	6,477,592	11/05/02	Chen et al.	710	52	
	AD	6,523,092	02/18/03	Fanning	711	134	
	AE	6,523,093	02/18/03	Bogin et al.	711	137	
	AF	6,622,227	09/16/03	Zumkehr et al.	711	167	
	AG	6,631,440	10/07/03	Jenne et al.	711	105	
	AH	2002/0144064	10/03/02	Fanning	711	144	
	AI	2003/0005223	01/02/03	Coulson et al.	711	118	
	AJ	2003/0229770	12/11/03	Jeddeloh	711	213	
	AK						
	AL						
	AM						
	AN						
	AO						
	AP						
	AQ						
	AR						
	AS						

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AT	Intel, "Intel 840 Chipset: 82840 Memory Controller Hub (MCH)", Datasheet, October 1999, pp. 1-178.
	AU	

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).